REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28						
REV STATUS OF SHEETS				REV																
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
93-03-26

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 2K X 9 BIDIRECTIONAL FIFO, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-92321**

SHEET 1 OF 29

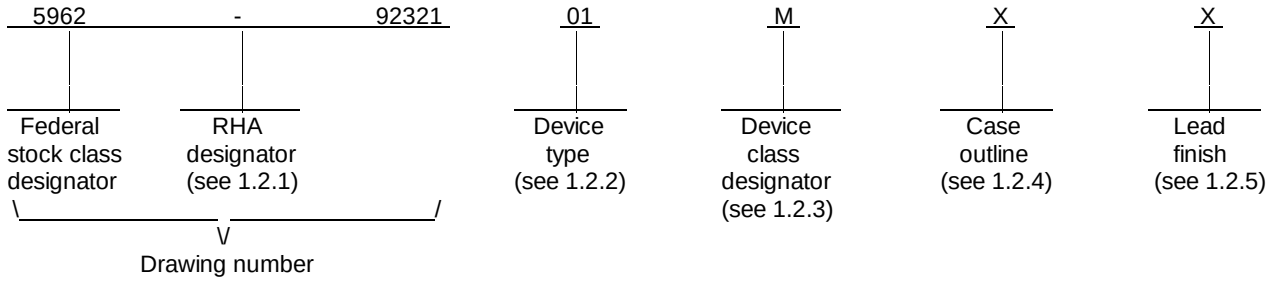
DESC FORM 193
JUL 91

5962-E040-93

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access Time
01		2K X 9-bit bidirectional FIFO	65 ns
02		2K X 9-bit bidirectional FIFO	40 ns
03		2K X 9-bit bidirectional FIFO	30 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or GDIP4-T28	28	Dual-in line
Y	GDFP2-F28	28	Flat pack
Z	CQCC1-N32	32	Rectangular leadless chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-BUL-103 (See 6.7.3 herein).

1.3 Absolute maximum ratings. 2/

Supply voltage range to ground potential (V_{CC})	-0.5 V dc to +7.0 V dc
DC voltage applied to the outputs in the high Z state	-0.5 V dc to +7.0 V dc
DC input voltage	-3.0 V dc to +7.0 V dc
Maximum power dissipation (P_D)	1.0 W 3/
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C
Temperature under bias	-55°C to +125°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Ground voltage (GND)	0 V dc
Input high voltage (V_{IH})	2.2 V dc minimum
Input low voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Logic testing for device classes Q or V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	4/ percent

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit case outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ Must withstand the added P_D due to short circuit test (e.g., I_{SC}).
4/ Values will be added when they become available.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Pennsylvania Street, N.W., Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. This is a full military detail specification and is suitable for qualification of device classes B and S to the requirements of MIL-M-38510. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.6 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-M-38510) shall be subjected to and pass the internal moisture content test at 5000 ppm (see method 1018 of MIL-STD-883). The frequency of the internal water vapor testing shall not be decreased unless approved by the preparing activity for class M or the qualifying activity for classes B and S. The TRB will ascertain the requirements as provided by MIL-I-38535 for classes Q and V. Samples may be pulled any time after seal.

3.3 Electrical performance characteristics and post irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post irradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S and V. All device class S devices shall be serialized in accordance with MIL-M-38510. Class V shall be serialized in accordance with MIL-I-38535.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -2.0 mA $V_{IN} = V_{IH}, V_{IL}$	1,2,3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8.0 mA $V_{IN} = V_{IH}, V_{IL}$	1,2,3	All		0.4	V
Input high voltage 1/	V_{IH}		1,2,3	All	2.2		V
Input low voltage 1/	V_{IL}		1,2,3	All		0.8	V
Input leakage current	I_{IX}	$V_{IN} = V_{CC}$ and GND	1,2,3	All	-10	+10	μA
Output leakage current	I_{OZ}	$\overline{STBX} \ge V_{IH}$ $V_{OUT} = V_{CC}$ and GND	1,2,3	All	-10	+10	μA
Output short circuit current 2/ 3/	I_{SC}	V_{CC} = 5.5 V, V_{OUT} = GND	1,2,3	All		-90	mA
Power supply current	I_{CC}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = 0 to 3.0 V, f = f_{MAX} 4/	1,2,3	01		145	mA
				02		160	
				03		170	
Standby current	I_{SB1}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, All inputs = V_{IH} min.	1,2,3	All		45	mA
Power down current	I_{SB2}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, All inputs = V_{CC} - 0.2 V	1,2,3	All		25	mA
Input capacitance 3/	C_{IN}	V_{CC} = 5.0 V, T = 25°C, f = 1 MHz, (see 4.4.1e)	4	All		8	pF
Output capacitance 3/	C_{OUT}	V_{CC} = 5.0 V, T = 25°C, f = 1 MHz (see 4.4.1e)	4	All		10	pF
Functional testing		See 4.4.1c	7,8	All			

See footnotes at end of table

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Read cycle time	t_{RC}	See figures 3 and 4 and note 5/	9,10,11	01	80		ns
				02	50		
				03	40		
Access time	t_A		9,10,11	01		65	ns
				02		40	
				03		30	
Read recovery time	t_{RR}		9,10,11	01	15		ns
				02,03	10		
Read pulse width	t_{PR}		9,10,11	01	65		ns
				02	40		
				03	30		
Read low to low-Z 3/ 6/	t_{LZR}		9,10,11	All	3		ns
Read high to data valid 3/ 7/	t_{DVR}		9,10,11	All	3		ns
Read high to high-Z 3/ 8/	t_{HZR}		9,10,11	01		30	ns
				02		25	
				03		20	
Write cycle time	t_{WC}		9,10,11	01	80		ns
				02	50		
				03	40		
Write pulse width	t_{PW}		9,10,11	01	65		ns
				02	40		
				03	30		
Write high to low-Z 3/ 6/	t_{HWZ}		9,10,11	All	10		ns
Write recovery time	t_{WR}		9,10,11	01	15		ns
				02,03	10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Data set-up time	t_{SD}	See figures 3 and 4 and note 5/	9,10,11	01	30		ns
				02	20		
				03	18		
Data hold time	t_{HD}		9,10,11	01	10		ns
				02,03	0		
$\overline{MR}$ cycle time	t_{MRSC}		9,10,11	01	80		ns
				02	50		
				03	40		
$\overline{MR}$ pulse width	t_{PMR}		9,10,11	01	65		ns
				02	40		
				03	30		
$\overline{MR}$ recovery time	t_{RMR}		9,10,11	01	15		ns
				02,03	10		
$\overline{STBX}$ high to $\overline{MR}$ high	t_{RPS}		9,10,11	01	65		ns
				02	40		
				03	30		
$\overline{BYPA}$ to $\overline{MR}$ high	t_{RPBS}		9,10,11	01	20		ns
				02	15		
				03	10		
$\overline{BYPA}$ hold after $\overline{MR}$ high	t_{RPBH}		9,10,11	All	0		ns
$\overline{MR}$ low to $\overline{BDA}$ high	t_{BDH}		9,10,11	01		80	ns
				02		50	
				03		40	
$\overline{STBX}$ high to $\overline{BYPA}$ low	t_{BSR}		9,10,11	01	15		ns
				02,03	10		

See footnotes at end of table

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
$\overline{MR}$ to $\overline{E}/\overline{F}$ low	t_{EFL}	See figures 3 and 4 and note 5/	9,10,11	01		80	ns
				02		50	
				03		40	
$\overline{MR}$ to $\overline{HF}$ high	t_{HFH}		9,10,11	01		80	ns
				02		50	
				03		40	
$\overline{BYPX}$ high to $\overline{STBX}$ low	t_{BRS}		9,10,11	01	15		ns
				02,03	10		
$\overline{STBX}$ low to $\overline{E}/\overline{F}$ low (read)	t_{REF}		9,10,11	01		60	ns
				02		35	
				03		30	
$\overline{STBX}$ high to $\overline{E}/\overline{F}$ high (read)	t_{RFF}		9,10,11	01		60	ns
				02		35	
				03		30	
$\overline{STBX}$ high to $\overline{E}/\overline{F}$ high (write)	t_{WEF}		9,10,11	01		60	ns
				02		35	
				03		30	
$\overline{STBX}$ low to $\overline{E}/\overline{F}$ low (write)	t_{WFF}		9,10,11	01		60	ns
				02		35	
				03		30	
$\overline{BYPX}$ high to $\overline{BDA}$ low (write)	t_{BDA}		9,10,11	01		60	ns
				02		35	
				03		30	
$\overline{BYPX}$ high to $\overline{BDA}$ high (read)	t_{BDB}		9,10,11	01		60	ns
				02		35	
				03		30	
$\overline{BYPX}$ low to data valid (read)	t_{BA}		9,10,11	01		60	ns
				02		40	
				03		30	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
$\overline{BYPX}$ high to high-Z (read) 3/ 8/	t_{BHZ}	See figures 3 and 4 and note 5/	9,10,11	01		30	ns
				02		25	
				03		20	
$\overline{STBX}$ high to $\overline{BYPX}$ low set-up	t_{TSB}		9,10,11	01	15		ns
				02,03	10		
$\overline{STBX}$ low after $\overline{BYPX}$ low	t_{TBS}		9,10,11	All	0	10	ns
$\overline{STBX}$ high recovery time	t_{TSN}		9,10,11	01	15		ns
				02,03	10		
$\overline{STBX}$ high to data high-Z 3/ 8/	t_{TSD}		9,10,11	01		30	ns
				02		25	
				03		20	
$\overline{BYPX}$ high recovery time	t_{TBN}		9,10,11	01	15		ns
				02,03	10		
$\overline{BYPX}$ high to data high-Z 3/ 8/	t_{TBD}		9,10,11	01		30	ns
				02		25	
				03		20	
$\overline{STBX}$ low to data valid	t_{TPD}		9,10,11	01		55	ns
				02		30	
				03		20	
Transparent propagation delay	t_{DL}		9,10,11	01		30	ns
				02		25	
				03		20	
$\overline{STBX}$ low to high-Z 3/ 8/	t_{ESD}		9,10,11	01		30	ns
				02		25	
				03		20	
$\overline{BYPX}$ low to high-Z 3/ 8/	t_{EBD}		9,10,11	01		30	ns
				02		25	
				03		20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
$\overline{STBX}$ high to low-Z 3/ 6/	t_{EDS}	See figures 3 and 4 and note 5/	9,10,11	01		30	ns
				02		25	
				03		20	
$\overline{BYPX}$ high to low-Z 3/ 6/	t_{EDB}		9,10,11	01		30	ns
				02		25	
				03		20	
$\overline{BYPX}$ pulse width (trans.)	t_{BPW}		9,10,11	01	65		ns
				02	40		
				03	30		
$\overline{STBX}$ pulse width (trans.)	t_{TSP}		9,10,11	01	55		ns
				02	30		
				03	20		
$\overline{BYPX}$ low to low-Z 3/ 6/	t_{BLZ}		9,10,11	All	10		ns
$\overline{BYPX}$ high to data invalid (read) 3/ 7/	t_{BDV}		9,10,11	All	3		ns
$\overline{STBX}$ low to $\overline{HF}$ low (write)	t_{WHF}		9,10,11	01		80	ns
				02		50	
				03		40	
$\overline{STBX}$ high to $\overline{HF}$ high (read)	t_{RHF}		9,10,11	01		80	ns
				02		50	
				03		40	
Effective read from write high	t_{RAE}		9,10,11	01		60	ns
				02		35	
				03		30	
Effective read pulse width after E/F high	t_{RPE}		9,10,11	01	65		ns
				02	40		
				03	30		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Effective write from read high	t_{WAF}	See figures 3 and 4 and note 5/	9,10,11	01		60	ns
				02		35	
				03		30	
Effective write pulse width after E/F high 3/	tWPF		9,10,11	01	65		ns
				02	40		
				03	30		
Bypass data set-up time	t_{BSU}		9,10,11	01	30		ns
				02	20		
				03	18		
Bypass data hold time	t_{BHL}		9,10,11	01	10		ns
				02,03	0		

1/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

2/ For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

3/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.

4/ At $f = f_{MAX}$, data inputs are cycling at the maximum frequency of $1/t_{RC}$.

5/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load in figure 3A unless otherwise noted.

6/ Transition is measured at $\pm$ 100 mV from the steady state on the output from the 1.5 level on the input, C_L = 5 pF (including scope and jig). See figure 3B.

7/ Transition is measured at the 1.5 V level on the output from the 1.5 V level on the input, C_L = 5 pF (including scope and jig). See figure 3B.

8/ Transition is measured at steady state high level -500 mV or steady state low level +500 mV on the output from the 1.5 V level on the input, C_L = 5 pF (including scope and jig). See figure 3B.

Device Types	All	
Case Outlines	X,Y	Z
Terminal Number	Terminal Symbol	
1	A_4	NC
2	A_3	A_4
3	A_2	A_3
4	A_1	A_2
5	A_0	A_1
6	$\overline{BYPA}$	A_0
7	GND	$\overline{BYPA}$
8	$\overline{BYP}B$	GND
9	BDA	$\overline{BYP}B$
10	B_0	BDA
11	B_1	B_0
12	B_2	NC
13	B_3	B_1
14	B_4	B_2
15	B_5	B_3
16	B_6	B_4
17	B_7	NC
18	B_8	B_5
19	$\overline{HF}$	B_6
20	$\overline{ST}BB$	B_7
21	MR	B_8
22	V_{CC}	$\overline{HF}$
23	$\overline{STB}A$	$\overline{ST}BB$
24	E/F	MR
25	A_8	V_{CC}
26	A_7	$\overline{STBA}$
27	A_6	NC
28	A_5	E/F
29	---	A_8
30	---	A_7
31	---	A_6
32	---	A_5

Figure 1. Terminal connections.

FIFO direction select

$\overline{MR}$	$\overline{BYPA}$	$\overline{BYPB}$	$\overline{STBA}$	$\overline{STBB}$	Action
1	X	X	X	X	Normal operation
⌐	1	1	1	1	FIFO direction A to B, registered bypass direction B to A
⌐	0	1	1	1	FIFO direction B to A, registered bypass direction A to B
0	X	X	X	X	Reset condition

Bypass operation truth table

Direction	$\overline{STBA}$	$\overline{BYPA}$	$\overline{STBB}$	$\overline{BYPB}$	Action
A→B	⌐⌙	1	⌐⌙	1	Normal FIFO operations, write at A, read at B
A→B	1	⌐⌙	⌐⌙	1	Normal FIFO read at B, bypass register read at A
A→B	⌐⌙	1	1	⌐⌙	Normal FIFO write at A, bypass register write at B
B→A	⌐⌙	1	⌐⌙	1	Normal FIFO operations, write at B, read at A
B→A	1	⌐⌙	⌐⌙	1	Normal FIFO write at B, bypass register write at A
B→A	⌐⌙	1	1	⌐⌙	Normal FIFO read at A, bypass register read at B
X	0	0	1	1	No FIFO operations, transparent data A to B
X	1	1	0	0	No FIFO operations, transparent data B to A

X = Don't care
1 = Logic 1 state
0 = Logic 0 state

⌐ = Rising edge

⌐⌙ = Low pulse

Figure 2. Truth table.

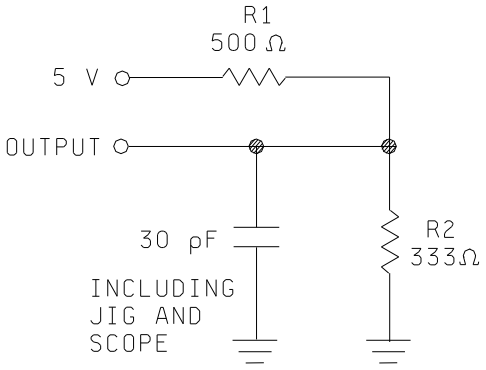
Exception conditions: operation not defined

Direction	$\overline{STBA}$	$\overline{BYPA}$	$\overline{STBB}$	$\overline{BYPB}$	Action
X	0	1	0	0	Data buses high impedance
X	1	0	0	0	Data buses high impedance
X	0	0	0	0	Data buses high impedance
X	0	0	1	0	Data buses high impedance
X	0	0	0	1	Data buses high impedance

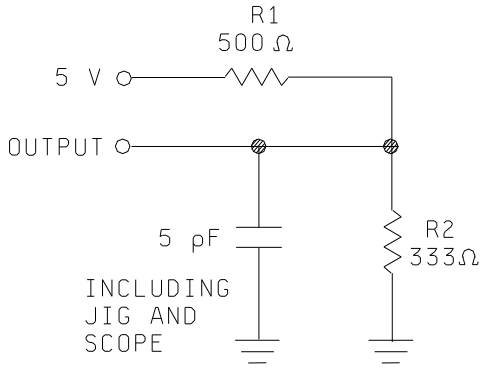
Flag truth table

$\overline{E}/\overline{F}$	$\overline{HF}$	State
0	1	Empty
1	1	1 - 1024 locations full
1	0	1025 - 2047 locations full
0	0	Full

Figure 2. Truth table - continued.



Circuit A
Output Load



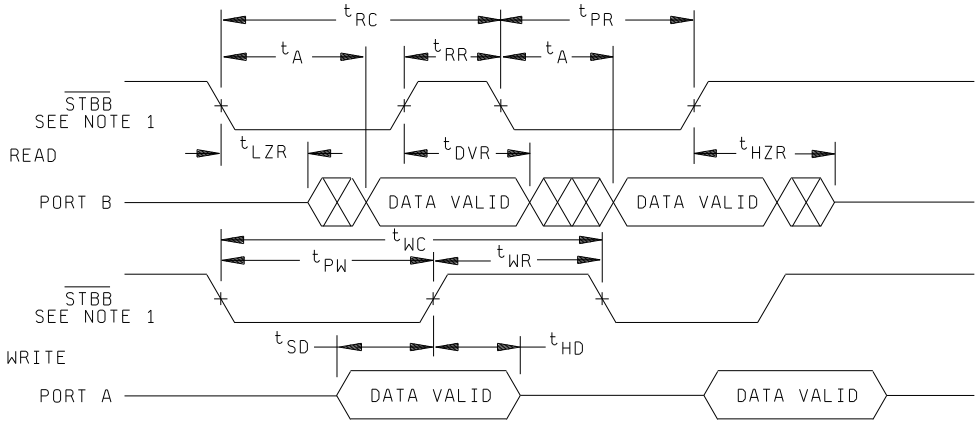
Circuit B
Output Load

AC test conditions

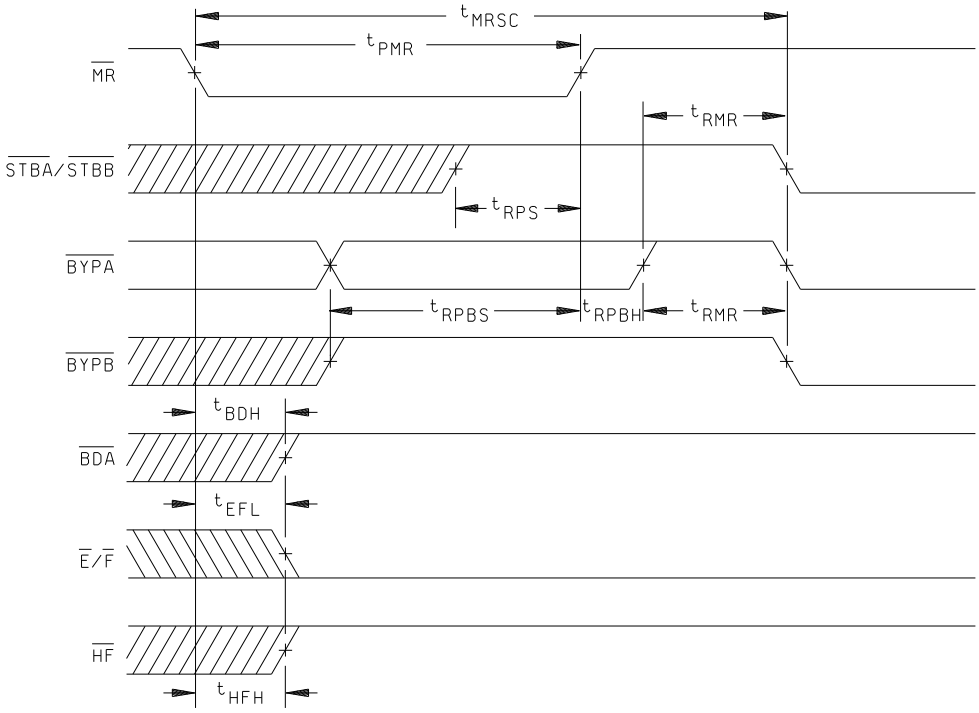
Input pulse levels	GND to 3.0 V
Input rise and fall levels	≤ 5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

Figure 3. Output load circuit and test conditions.

Asynchronous read and write timing diagram



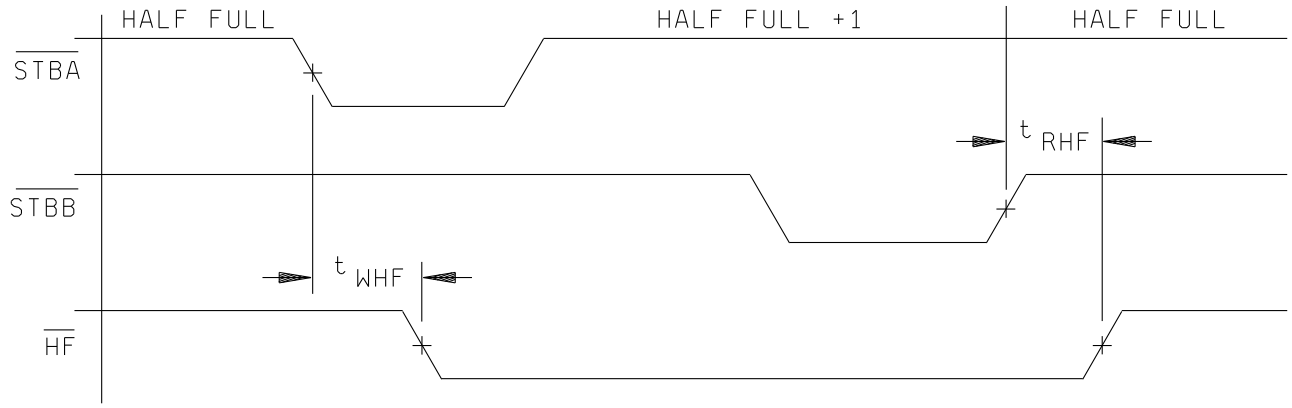
Master reset timing diagram



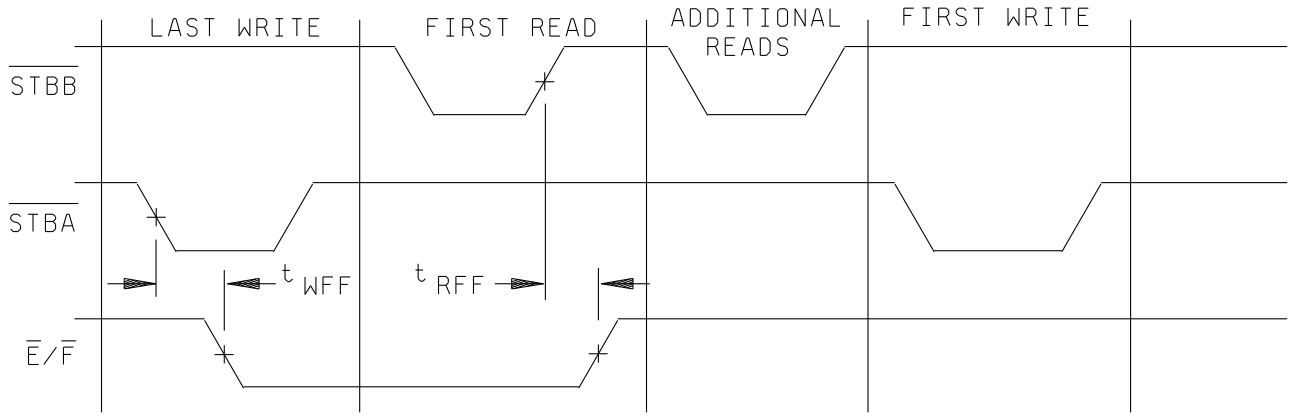
NOTES:
1. Direction selected as Port A to Port B.

FIGURE 4. Switching waveforms.

Half-full flag timing diagram (See note 1)



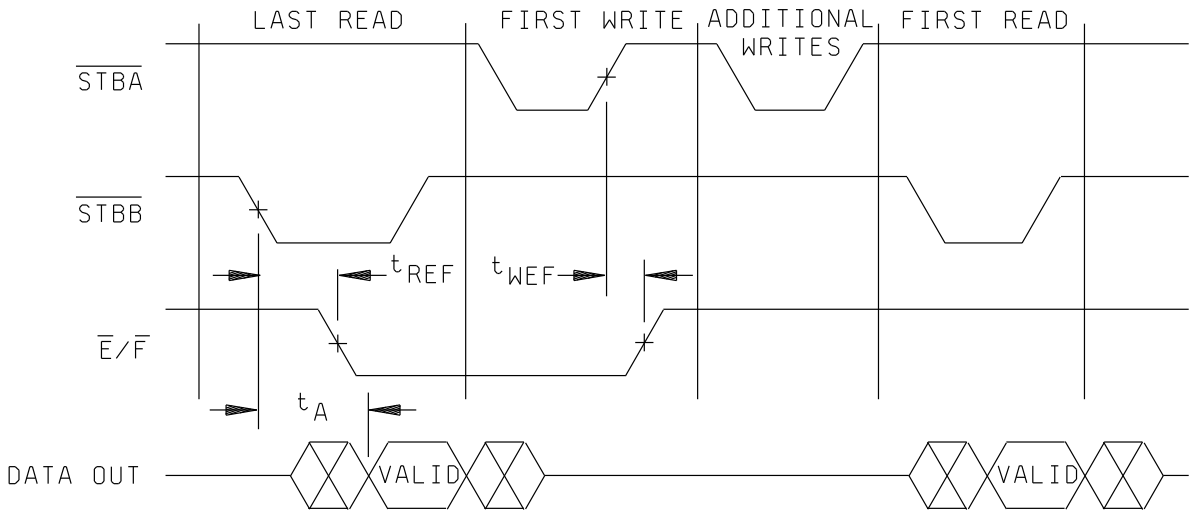
Last write to first read empty/full flag timing diagram (See note 1)



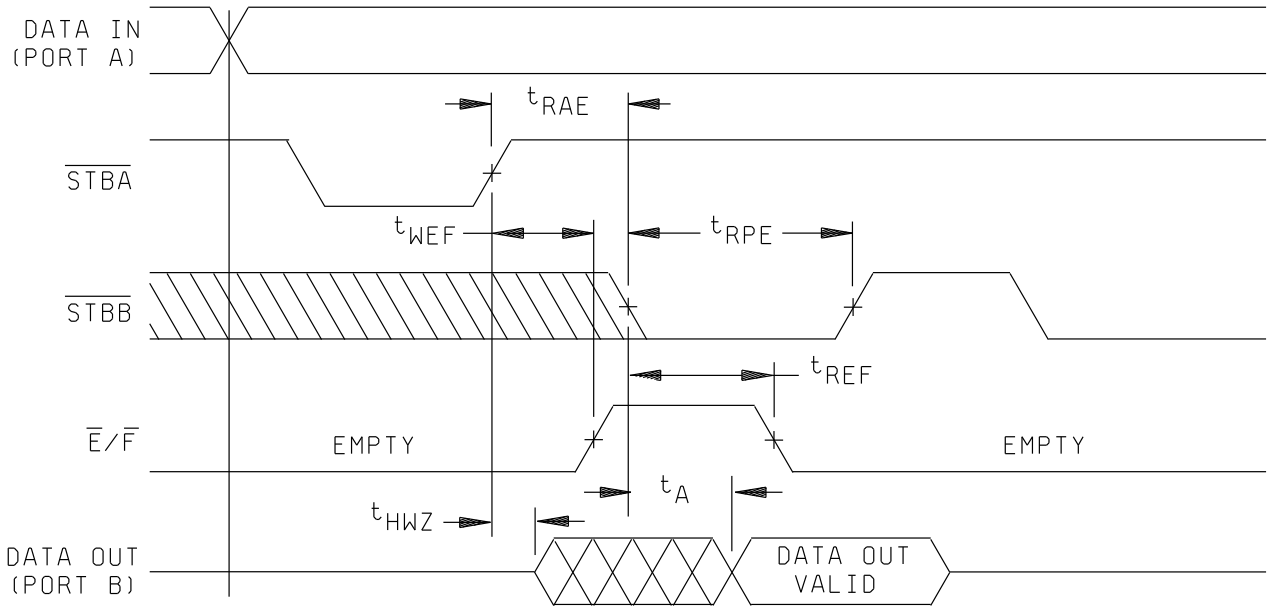
NOTES:
1. Direction selected as A to B

FIGURE 4. Switching waveforms - continued.

Last read to first write empty/full flag timing diagram (See note 1)



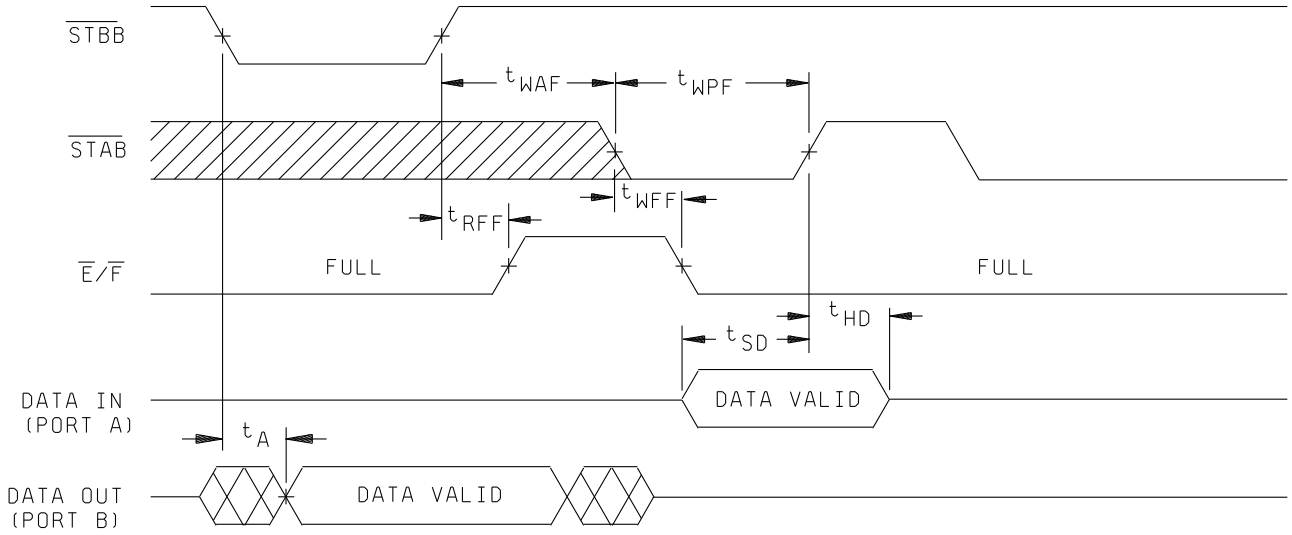
Empty/full flag and read bubble-through mode timing diagram (See note 1)



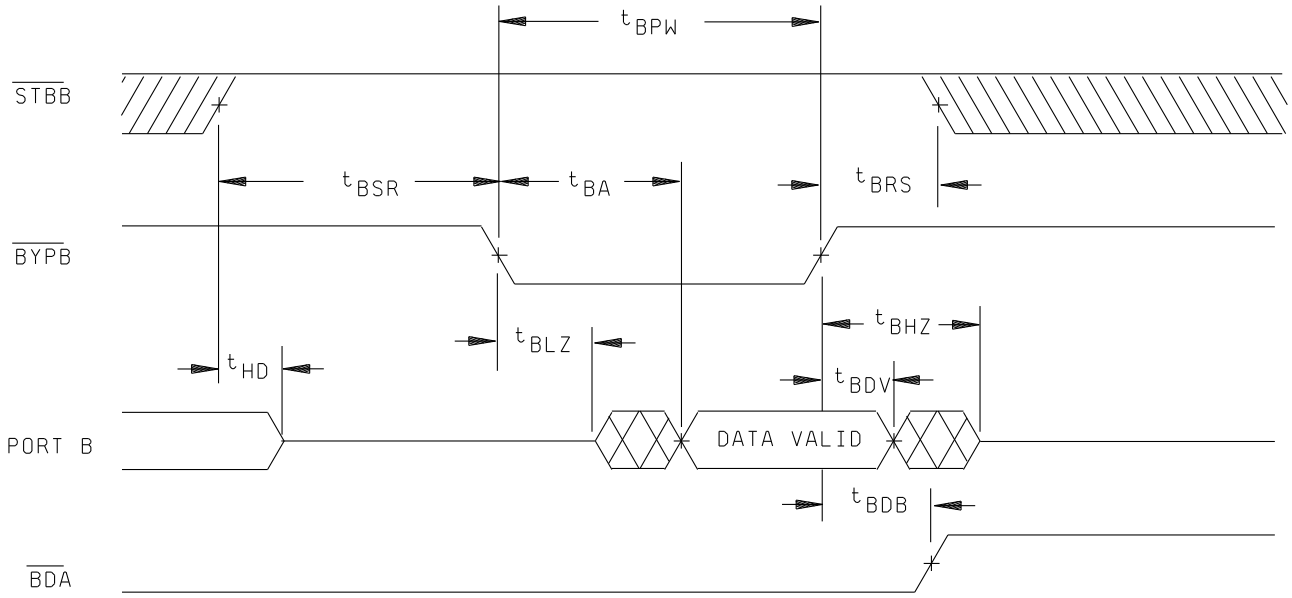
NOTES:
1. Direction selected as A to B

FIGURE 4. Switching waveforms - continued.

Empty/full flag and write bubble-through mode timing diagram (See note 1)



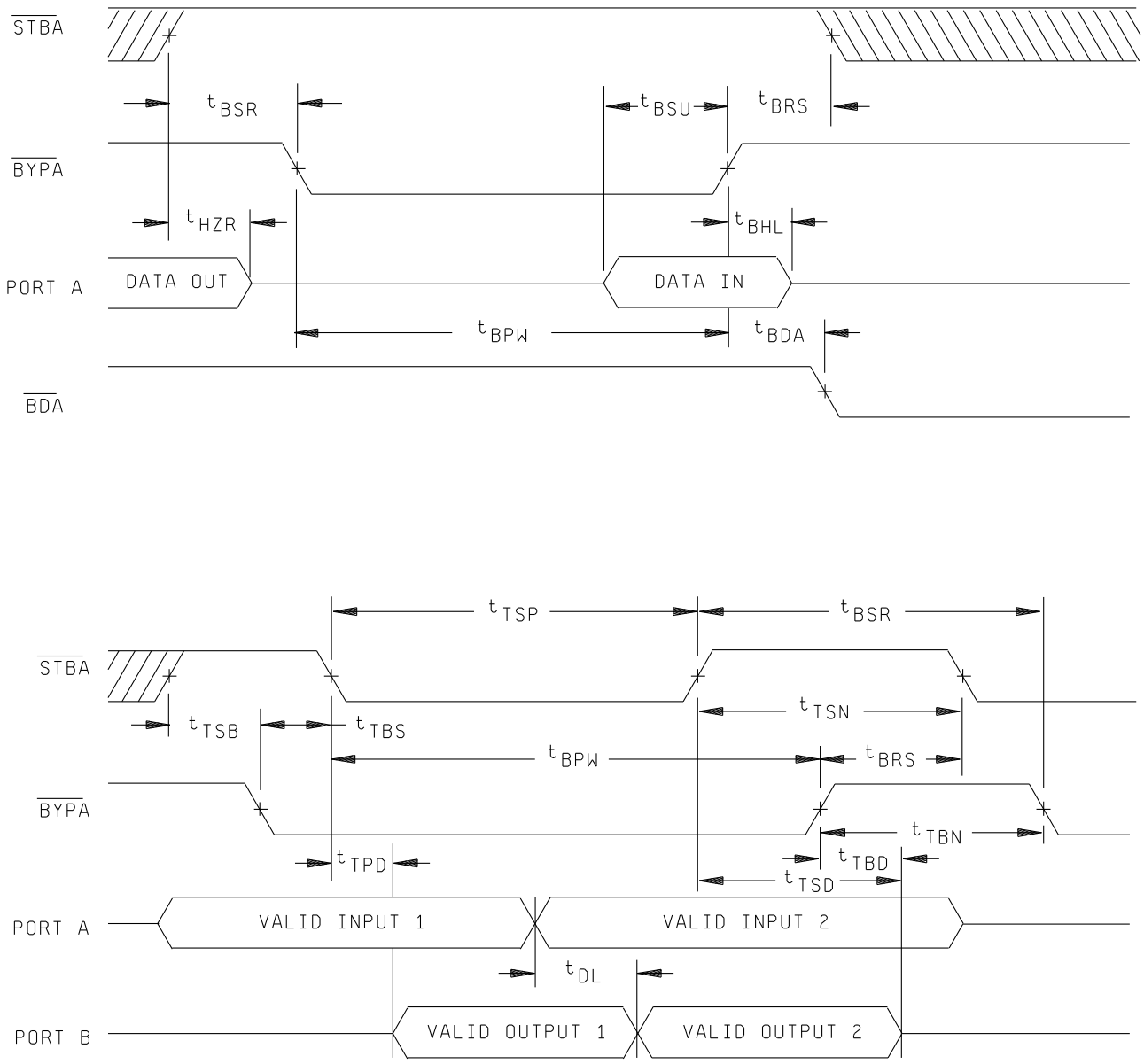
Registered bypass read timing diagram (See note 2)



NOTES:
1. Direction selected as A to B
2. Port B selected to read bypass register (FIFO direction Port B to Port A).

FIGURE 4. Switching waveforms - continued.

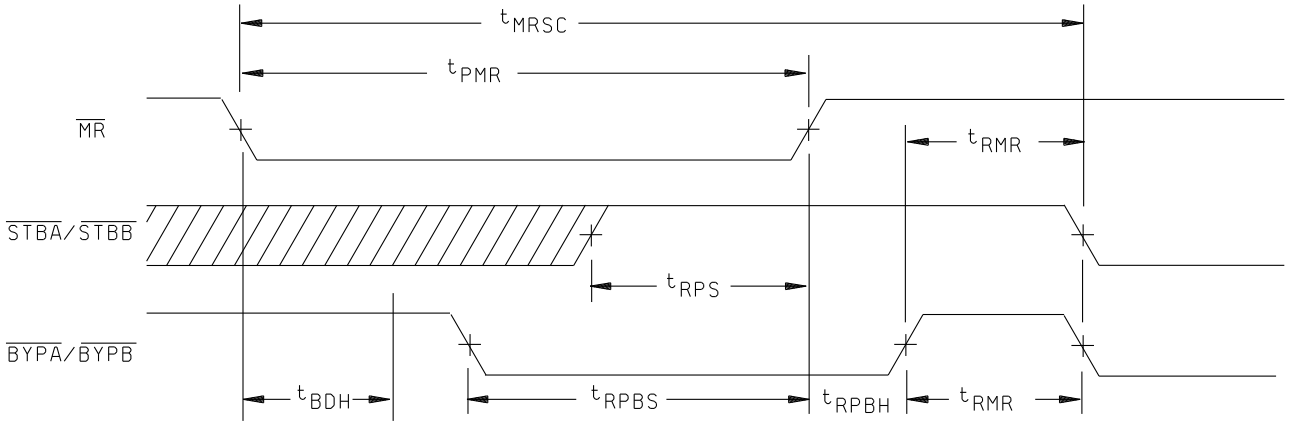
Registered bypass write timing diagram (See note 1)



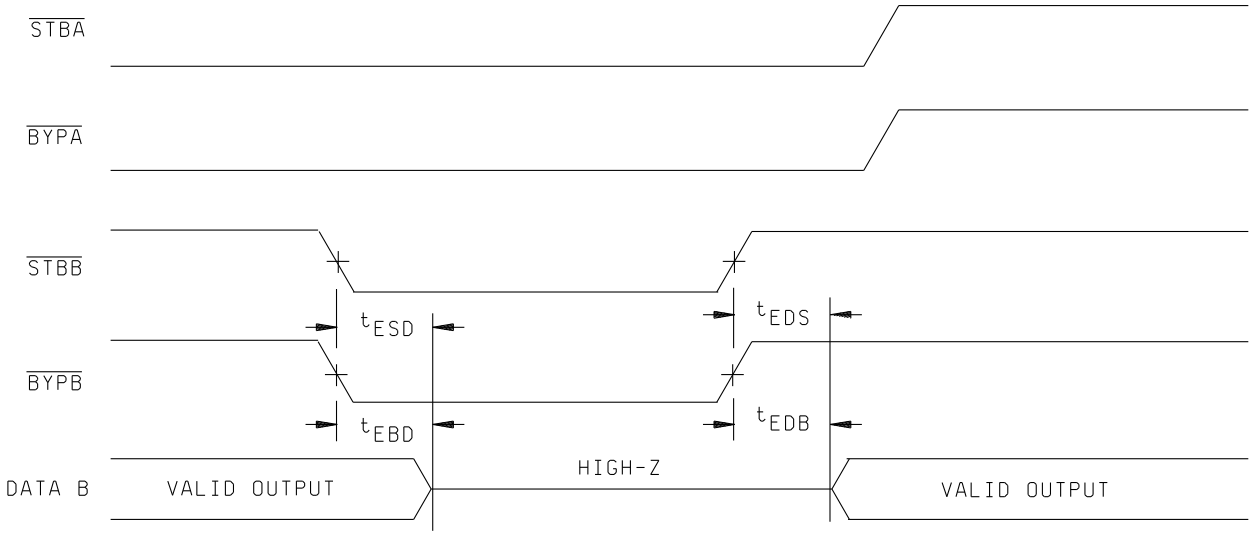
NOTES:
1. Port A selected to write bypass register (FIFO direction Port B to Port A).
2. Diagram shows transparent bypass initiated by Port A. Times are identical if initiated by Port B.

FIGURE 4. Switching waveforms - continued.

Test mode timing diagram



Exception condition timing diagram (See note 1)



NOTES:
1. Diagram shows transparent bypass initiated by Port A. Times are identical if initiated by Port B.

FIGURE 4. Switching waveforms - continued.

4.2.1 Additional criteria for device classes M, B, and S (Continued).

(1) Static burn-in for device class S (method 1015 of MIL-STD-883, test condition A).

(a) All inputs shall be connected to GND. Outputs may be open or connected to 4.5 V minimum. Resistors R1 are optional on both inputs and outputs, and required on outputs connected to V_{CC} ±0.5 V. R1 = 220Ω to 47 kΩ. For static II burn-in, reverse all input connections (i.e., V_{SS} to V_{CC}).

(b) V_{CC} = 4.5 V minimum.

(c) Ambient temperature (T_A) shall be +125°C minimum.

(d) Test duration for the static test shall be 48 hours minimum. The 48-hour burn-in shall be broken into two sequences of 24 hours each (static I and static II) followed by interim electrical measurements.

(1) Static burn-in for device class S (method 1015 of MIL-STD-883, test condition A).

(a) All inputs shall be connected to GND. Outputs may be open or connected to 4.5 V minimum. Resistors R1 are optional on both inputs and outputs, and required on outputs connected to V_{CC} ± 0.5 V. R1 = 220Ω to 47 kΩ. For static II burn-in, reverse all input connections (i.e., V_{SS} to V_{CC}).

(b) V_{CC} = 4.5 V minimum.

(c) Ambient temperature (T_A) shall be +125°C minimum.

(d) Test duration for the static test shall be 48 hours minimum. The 48-hour burn-in shall be broken into two sequences of 24 hours each (static I and static II) followed by interim electrical measurements.

(2) Dynamic burn-in for device classes M, B, and S (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

d. For classes S and B devices, post dynamic burn-in electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition, and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.2.3 Percent defective allowable (PDA).

a. The PDA for class S devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.

b. The PDA for class B devices shall be in accordance with MIL-M-38510 for dynamic burn-in.

c. Static burn-in I and II failures shall be cumulative for determining PDA.

4.2.3 Percent defective allowable (PDA).(Continued)

d. Those devices whose measured characteristics, after burn-in, exceed the specified delta limits or electrical parameter limits specified in table I, subgroup 1, are defective and shall be removed from the lot. The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA.

e. The PDA for device classes Q and V shall be in accordance with MIL-I-38535 for dynamic burn-in.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Qualification data for subgroup 7, 8A, and 8B shall be attributes only.

4.3.1.1 Qualification extension for device classes B and S. When authorized by the qualifying activity, if a manufacturer qualifies one device type which is identical (i.e., same die) to other device types on this specification, the slower device types may be part I qualified, upon the request of the manufacturer, without any further testing. The faster device types may be part I qualified by performing only group A qualification testing.

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device. These tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes B and S, the procedures and circuits shall be maintained under document revision control by the manufacturer and shall be made available to the qualifying activity upon request. For device classes Q and V, the procedures and circuits shall be shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC standard number 17 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein. For device class S steady-state life tests, the test circuit shall be submitted to the qualifying activity.

a. For device class S, steady-state life test circuits shall be conducted using test condition D and the circuit described in 4.2.1b herein, or equivalent as approved by the qualifying activity.

b. For device class S only, end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 5 of group B inspections and shall consist of tests specified in table IIB herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIB herein.

4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B, the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3.1 Additional criteria for device classes M and B.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device classes B, S, Q, and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

(This section contains information of general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Symbols, definitions, and functional descriptions.

C_{IN}	Input terminal capacitance.
C_{OUT}	Output terminal capacitance.
GND	Ground zero voltage potential.
I_{CC}	Supply current.
I_{IX}	Input current.
IOZ	Output current.
T_C	Case temperature.
V_{CC}	Positive supply voltage (5.0 V).
A_{0-8}	I/O data port associated with $\overline{\text{BYPA}}$ and $\overline{\text{STBA}}$.
B_{0-8}	I/O data port associated with $\overline{\text{BYPB}}$ and $\overline{\text{STBB}}$.
$\overline{\text{BYPA}}$	Input to registered bypass mode select for A side.
$\overline{\text{BYPB}}$	Input to registered bypass mode select for B side.
$\overline{\text{BDA}}$	Output from bypass data available flag.
$\overline{\text{STBA}}$	Input to data strobe for A side.
$\overline{\text{STBB}}$	Input to data strobe for B side.
$\overline{\text{E}}/\overline{\text{F}}$	Output from encoded empty/full flag.
$\overline{\text{HF}}$	Output from half full flag.
$\overline{\text{MR}}$	Input to master reset.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroup (in accordance with MIL-STD-883, method 5005, table I)			Subgroups (in accordance with MIL-I-38535, table III)	
		Device class M	Device class B	Device class S	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)	- - -	1, 7 9	1, 7 9	1, 7 9	1, 7 9
2	Static burn-in I and II (method 1015)	Not required	Not required	Required	Not required	Required
3	Same as line 1			1*, 7* △		1*, 7* △
4	Dynamic burn_in (method 1015)	Required	Required	Required	Required	Required
5	Same as line 1			1*, 7* △		1*, 7* △
6	Final electrical parameters	1*, 2, 3, 7*, 8A 8B, 9, 10, 11	1*, 2, 3, 7*, 8A 8B, 9, 10, 11	1*, 2, 3, 7*, 8A 8B, 9, 10, 11	1*, 2, 3, 7*, 8A 8B, 9, 10, 11	1*, 2, 3, 7*, 8A 8B, 9, 10, 11
7	Group A test requirements	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group B end-point electrical parameters			1, 2, 3, 7, 8A, 8B, 9, 10, 11 △		
9	Group C end-point electrical parameters	2, 3, 7 8A, 8B	1, 2, 3, 7 8A, 8B △		1, 2, 3, 7 8A, 8B △	1, 2, 3, 7 8A, 8B △
10	GroupD end-point electrical parameters	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
11	Group E end-point electrical parameters	1, 7, 9	1, 4, 7, 9	1, 4, 7, 9	1, 4, 7, 9	1, 4, 7, 9

1/ Blank spaces indicate tests are not applicable.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7 and 8 functional tests shall verify the truth table.

4/ * indicates PDA applies to subgroup 1 and 7.

5/ ** see 4.4.1e.

6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).

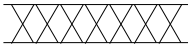
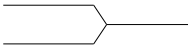
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{SBI} standby	±10% of specified value in table I
I_{IX}, I_{OZ}	±10% of specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memery are specified from the device point of view. Thus, the accesss time is shown as a maximum since the device never provides data later than that time.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), who was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can procure to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

6.6 One part - one part number system. (continued)

Military documentation format	Example PIN under new system	Manufacturing source listing	Document
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY (Part 1 or 2)	QPL-38510	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 93-03-26

Approved sources of supply for SMD 5962-92321 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9232101MXX	65786	CY7C439-65DMB
5962-9232101MYX	65786	CY7C439-65KMB
5962-9232101MZX	65786	CY7C439-65LMB
5962-9232102MXX	65786	CY7C439-40DMB
5962-9232102MYX	65786	CY7C439-40KMB
5962-9232102MZX	65786	CY7C439-40LMB
5962-9232103MXX	65786	CY7C439-30DMB
5962-9232103MYX	65786	CY7C439-30KMB
5962-9232103MZX	65786	CY7C439-30LMB

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65786	Cypress Semiconductor 3901 North First Street San Jose, CA 951